DOI: https://doi.org/10.15276/aait.09.2026.45
UDC 004.052

Structural analysis of ambiguity emergence scenarios in self-testing of fault-tolerant multiprocessor systems

Vitaliy A. Romankevich[1)]
ORCID: https://orcid.org/0000-0003-4696-5935; zavkaf@scs.kpi.ua. Scopus Author ID: 57193263058
Oleksandr O. Melnyk[1)]
ORCID: https://orcid.org/0009-0003-7527-8146; inboxnumberzero@zoho.com
Alexei M. Romankevich[1)]
ORCID: https://orcid.org/0000-0001-5634-8469; romankev@scs.kpi.ua. Scopus Author ID: 6602114176
Kostiantyn V. Morozov[1)]
ORCID: https://orcid.org/0000-0003-0978-6292; mcng@ukr.net. Scopus Author ID: 57222509251
Lefteris Zacharioudakis[2)]
ORCID: https://orcid.org/0000-0002-9658-3073; l.zacharioudakis@nup.ac.cy. Scopus Author ID: 57422876200
[1)] National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute", 37, Beresteiskyi Ave, Kyiv, 03056, Ukraine
[2)] Neapolis University Pafos, 2, Danais Ave., Pafos, 8042, Cyprus

ABSTRACT

The relevance of the study is determined by the need to improve the reliability and efficiency of self-testing procedures for fault-tolerant multiprocessor systems. Existing approaches based on a minimal set of diagnostic connections may leave some processor states unresolved, requiring additional tests. **The aim** is to refine the structural description of ambiguity formation in systems whose diagnostic graph is a strongly connected directed circulant with two jumps. **The objectives** include deriving new restrictions on ?-chains and ?-subgraphs, determining conditions for the existence of such subgraphs with the minimum admissible number of incoming fault links, and establishing when several independent subgraphs can arise. **Methods.** Graph-theoretic analysis, modular relations for circulant parameters, structural decomposition of ambiguity regions, and analysis of admissible ?-chain configurations are used. **The results** establish a finite upper bound on ?-chain length for the considered unresolved-fault state. It is proved that a ?-subgraph with the minimum admissible number of incoming fault links can contain only one processor whose state remains unresolved. A necessary relation between circulant jumps allowing two independent ?-subgraphs of this type to coexist is also established. **The scientific novelty** lies in extending the structural theory of ambiguity formation for the considered number of faults and substantially narrowing the set of configurations requiring further analysis. **The practical value** of the results consists in their applicability in refining self-testing algorithms, excluding impossible ambiguity configurations, and reducing additional diagnostic checks required to resolve uncertain processor states.

Keywords: fault-tolerant multiprocessor system; self-testing; diagnostic graph; directed circulant; ambiguous processor state

For citation: **Romankevich V. A., Melnyk O. O., Romankevich A.M., Morozov K. V., Zacharioudakis Lefteris. "Structural analysis of ambiguity emergence scenarios in self-testing of fault-tolerant multiprocessor systems". 2026; Vol.9 No.4: 699–711. DOI: https://doi.org/10.15276/aait.09.2026.45**

INTRODUCTION

Multiprocessor computer systems are widely used in modern control systems, including those responsible for controlling critical facilities [1], [2], [3], [4], [5], [6]. Failures of such systems may result in substantial losses, including loss of human life, and are therefore clearly unacceptable. Consequently, reliable and efficient self-testing and timely fault detection in control systems [7], [8], [9], [10] particularly in aerospace applications [11], [12], [13], [14], [15], [16] remain an important and relevant problem.

Given the strict reliability requirements, any improvement in the efficiency of self-testing procedures for fault-tolerant multiprocessor systems (FTMS) must, first and foremost, ensure full functional equivalence, that is, an equal or better outcome (complete determination of the states of all of the system's processors). Therefore, avoiding ambiguities – processors whose states remain unresolved even after the testing procedure has been completed – is a feature of critical importance for any proposed FTMS testing method.

Methods have already been proposed for improving the efficiency of FTMS testing, particularly through the use of a minimum number of interprocessor connections [17]. However, since reducing the number of connections available for testing inevitably leads to ambiguities in certain system topologies and fault arrangements, resolving these ambiguities requires additional connections and, consequently, adjusting the design of systems for more connections than would be necessary under ideal conditions. This significantly limits the practical potential for improving the efficiency of FTMS testing.

© Romankevich V., Melnyk O., Romankevich A., Morozov K., Zacharioudakis Lefteris, 2026

This is an open access article under the CC BY license (https://creativecommons.org/licenses/by/4.0/deed.uk)

Determining the conditions under which ambiguities may arise depending on the system topology and parameters (henceforth "configuration") would make it possible to avoid, already at the design stage, certain configurations that permit a relatively large number of ambiguities. This would improve testing efficiency and bring it closer to the ideal case. The investigation of such conditions is therefore a promising direction within the broader problem of FTMS self-testing.

LITERATURE REVIEW AND PROBLEM STATEMENT

General conditions for the FTMS diagnosability have already been established [18]. The Preparata–Metze–Chien model (PMC model) is widely recognized and serves as the theoretical foundation for numerous methods of FTMS testing [19], [20], [21]. The PMC model represents an FTMS in the form of a diagnostic graph and therefore makes it possible to apply graph-theoretic tools and methods to the investigation of self-testing problems. The model also establishes the fundamental constraints of the problem. In particular, the admissible number of faulty processors (T) in a given FTMS is restricted by the condition $n \geq 2T + 1$, where n denotes the total number of processors in the system, or, equivalently, the order of its diagnostic graph.

In many cases, the parameter T plays a central role in the formulation and solution of the testing problem. An FTMS is generally designed with a particular expected level of fault tolerance or structural redundancy in mind, which makes it possible to determine the admissible number of processor faults in a relatively straightforward and transparent manner [22], [23], [24], [25].

A promising direction in the study of FTMS self-testing is associated with the application of circulant graphs as FTMS diagnostic graphs, and employment of their structural and algebraic properties [26]. In particular, an FTMS testing method relying on the minimum possible number of interprocessor connections has been proposed using precisely this approach [17]. It has been noted that the application of this method may result in ambiguities, which must subsequently be resolved locally through the use of additional connections. It was shown that, nevertheless, there exist system configurations in which the number of possible ambiguities is fundamentally bounded, regardless of the particular arrangement of the faulty processors and test results. For example, in certain topologies no more than one ambiguity may arise when $T = 3$, while no more than two ambiguities may arise when $T = 4$.

Topologies that allow a larger number of ambiguities, potentially reaching $T - 1$, have been demonstrated in [27].

Sufficient conditions for the occurrence of such cases have also been established: $3S_1 \equiv 3S_2 \bmod n$ for $T = 4$, and $2S_1 \equiv 2S_2 \bmod n$ for $T = 3$, where S_1 and S_2 denote the jumps of the circulant diagnostic graph.

The fundamental conditions governing the occurrence of ambiguities and the formation of the associated substructures, referred to as ?-subgraphs and ?-chains, were investigated in [28]. The principal concepts and results of that study, which form the basis for the present work, are summarized below.

The following notation was introduced. The state of a processor is denoted as 0 if the processor is functional, as 1 if it is faulty, and as ? if its state remains unresolved (ambiguous). Accordingly, the term 0-processor denotes a processor in state 0, whereas a 1-connection denotes a connection outgoing from a processor in state 1. A connection associated with a particular test result, as opposed to a connection outgoing from a processor in a particular state, may be denoted as a "connection '1'," and similar notation may be used for other test results. The quantities n_1, n_0, and $n_?$ denote the numbers of processors in the corresponding states. The parameter T^* denotes the number of admissible faults at a particular stage of the diagnostic procedure. The quantity w_i denotes the weight of processor i; a detailed explanation of the role played by processor weights in the testing procedure is provided in [17] and [28].

The concept of a "?-subgraph" was also introduced. A ?-subgraph is defined as the maximal connected subgraph of the FTMS diagnostic graph that contains a particular ?-vertex and consists exclusively of ?-vertices. The number of incoming arcs of a ?-subgraph – that is, arcs entering the vertices of the ?-subgraph from vertices that do not belong to it – is denoted by d^u. Such incoming arcs are always 1-connections.

The concept of a "?-chain" was introduced in a similar manner. A ?-chain is the maximal chain formed by arcs corresponding to a particular jump, containing a given ?-vertex and consisting exclusively of ?-vertices.

The following theorems were formulated and proved (the numbering is given in the order in which the theorems are cited below and does not correspond to their original numbering in [28]):

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

Theorem 1. The occurrence of ?-processors is impossible in an FTMS with one 1-processor or less.

Theorem 2. The occurrence of a ?-subgraph with $d^u \leq 1$ is impossible.

Theorem 3. The occurrence of $n_? > n_1$ is impossible when $n_1 = T - 1$.

Theorem 4. The occurrence of a ?-subgraph with two incoming 1-connections originating from the same single 1-processor is impossible.

Considering the results obtained in the previous studies, it follows directly that ambiguities cannot occur when $T \leq 2$, as established by **Theorem 1**. When $T = 3$, the number of ambiguities $n_?$ is bounded by the $n_? \leq 2$ condition. Indeed, **Theorem 1** requires the presence of at least two 1-processors for any ?-processors to occur, whereas **Theorem 3** establishes that the number of ?-processors cannot exceed the number of 1-processors.

For the $T = 4$ case, these results imply that the behavior of the system is already known for most possible values of n_1:

- $n_1 \leq 1 \rightarrow n_? = 0$ (**Theorem 1**).
- $n_1 = 4 = T \rightarrow n_? = 0$ (since, when all 1-processors have been identified, the state of the entire system is fully determined).
- $n_1 = 3 = T - 1 \rightarrow n_? \leq 3$ (**Theorem 3**).

Therefore, the following general relation may be written:

$$T = 4, n_1 \neq 2 \rightarrow n_? \leq 3.$$

To summarize, the previous studies established the foundations for the structural analysis of ambiguities that may arise in constructively regular diagnostic graphs of FTMS. They introduced the principal theoretical concepts and proved a number of propositions restricting the conditions under which such ambiguities and their associated substructures may occur.

Nevertheless, the case $T = 4$ has not yet been described completely. In particular, it has not been established whether the number of ambiguities may be equal to or greater than *T*, either in this specific case or in the general case, depending on the particular parameters and structural characteristics of an FTMS.

Thus, the objective of this study is to continue the investigation of the case $T = 4$, specifically the configurations characterized by $T = 4$ and $n_1 = 2$, and specifically the $d^u = 2$?-subgraphs within those configurations. The obtained results are intended to bring the description of this case closer to completion and to expand the theoretical and practical tools available for addressing ambiguities in the design of FTMSs and their self-testing procedures. The case $T = 4$ is of particular practical importance, since real-world applications commonly impose the requirement $T \leq 4$, whereas larger values of T are rarely used in practice. Simultaneously, the cases characterized by $T < 4$ have already been investigated in considerable detail in previous studies.

It should be noted that this line of research does not propose an alternative method for evaluating FTMS diagnosability, but instead investigates the structural conditions under which unresolved processor states may arise within the considered self-testing method.

METHODS AND LIMITATIONS

Let us first establish the basic conditions and assumptions of the problem under consideration. The present study considers only fault-tolerant multiprocessor systems whose diagnostic graph $G(n, S_1, S_2)$ is a strongly connected directed circulant of order n with jumps S_1 and S_2, that is, $\gcd(n, S_1, S_2) = 1$. Furthermore, under the conditions of the PMC model [18], the admissible number of faults T is constrained by the requirement $n \geq 2T + 1$. Such a graph may contain neither multiple arcs, reciprocal arcs, nor self-loops.

To simplify the analysis, processors, corresponding to the vertices of the diagnostic graph, will be denoted by their indices $(0, 1, \ldots, n - 1)$ whenever necessary. Since the diagnostic graph is a circulant, vertex 0 may be selected arbitrarily without loss of generality. Accordingly, the predecessors of processor i have the indices $i - S_1$ and $i - S_2$, whereas its successors have the indices $i + S_1$ and $i + S_2$. All operations on processor indices are performed modulo *n*.

The testing method with the minimum number of connections [17] relies on the sequential analysis of the weight of each processor, together with the test results assigned to the arcs of the diagnostic graph. The principal provisions of this method may be summarized as follows:

- If the diagnostic graph contains an arc $v_{ij} = 1$, then the set of processors $\{i, j\}$ contains at least one 1-processor; in other words, at least one of these two processors is faulty. This makes it possible to exclude both processors, considered as the pair (i, j), from further analysis at a particular stage of the testing procedure while decreasing T^* by one. For brevity, such a pair of processors will henceforth be referred to as a "1-pair."
- The state of a processor i whose weight satisfies the condition $w_i > T^*$ is determined to be 0, meaning that the processor is functional.

- If the state of processor j has already been determined, while the test result associated with the incoming arc from its predecessor i does not correspond to this known state, the state of processor i is determined to be 1, meaning that the processor is faulty.

In the figures, the following notation will be used whenever it is necessary to illustrate a particular configuration or diagnostic case:

- The actual state of a processor, which is not available to the testing procedure, is represented by color: green denotes a functional processor, whereas red denotes a faulty processor.
- The index (or another unique identifier of a processor) is shown in the center of the corresponding vertex.
- The processor state determined by the testing procedure, namely 0, 1, or ?, is indicated next to the corresponding vertex.
- The test result associated with a particular connection (arc), either 0 or 1, is shown directly on that connection.
- The jump by which a particular connection is formed is indicated next to the connection.

The principal methodology used for the structural analysis of ambiguities consists in first determining the restrictions specific to the case under investigation and then constructing all possible configurations of ?-subgraphs by exhaustive combinatorial enumeration under these initial restrictions. The enumeration is considered complete when all permitted configurations have been generated.

For each structurally distinct configuration, the mathematical conditions required for its existence are derived, with particular attention being paid to the relationships among the predecessors and successors of its processors. These conditions are subsequently reduced to a minimal or otherwise simplified form and compared both with one another and with the fundamental assumptions of the problem.

Any contradiction identified during this comparison indicates that the corresponding configuration is impossible under the established conditions. Conversely, if no contradiction is found, the resulting simplified condition constitutes a useful and unambiguous result describing the circumstances under which the considered configuration may exist.

RESEARCH RESULTS

For the $T = 4$, $n_1 = 2$ case, the system contains four available 1-connections, since each 1-processor provides two such connections. In addition, because two distinct 1-processors are present, the occurrence of so-called xx-processors becomes possible. These are ?-processors both of whose incoming connections are 1-connections [17].

Throughout the analysis, the concepts of ?-subgraphs and ?-chains will be used. As is known from [28], each ?-processor belongs to two ?-chains, $c(S_1)$ and $c(S_2)$. For the sake of brevity and improved clarity, the ?-chain $c(S_1)$ will be denoted as L (and its processors as L_0, L_1, and so forth), whereas $c(S_2)$ will be denoted as R. It is also known that the predecessor of the first processor of a ?-chain must always be either a 1-processor or the last processor of the same chain; in the latter case, the ?-chain is a cycle.

Let us now formulate a theorem that will be important for the subsequent analysis and that restricts the possible length of ?-chains.

Theorem 5. The length $l(c)$ of a ?-chain c is bounded as $1 \le l(c) \le 4$ for $T^* = 2$.

Proof. The lower bound $l(c) = 1$ is obvious. It is illustrated by the case of a ?-subgraph consisting of a single vertex (Fig. 1), which may arise in any FTMS configuration satisfying the imposed conditions:

$$L: [X_0] \to L_0$$
$$R: [X_1] \to R_0$$
$$L_0 = R_0.$$

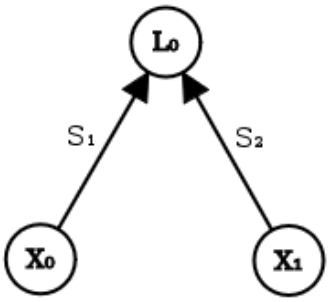


Fig. 1. **A single-vertex ?-subgraph**
Source: **compiled by the authors**

The upper bound can be estimated by analyzing the possible weights of processors belonging to a ?-chain. The condition $T^* = 2$ means that the state of any processor i with weight $w_i > T^*$, that is, $w_i \ge 3$, will be determined as functional (0).

The value $w_i = 3$ is obtained in the case of two consecutive connections with test result "0":

$$\underset{1}{\left[X \overset{1}{\to}\right]} L_0 \overset{0}{\to} \underset{2}{L_1} \overset{0}{\to} \underset{3}{L_2},$$

where the test results are indicated above the connections and the processor weights are indicated below them. In the example shown, the state of L_2 is

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

determined as functional, and the ?-chain of length 2 includes only the processors L_0 and L_1. Consequently, a ?-chain with $l > 2$ can arise only in the presence of connections with test result "1", which interrupt longer sequences of "0" arcs and therefore prevent the occurrence of $w_i \geq 3$.

However, the occurrence of even a single connection with test result "1" makes it possible to exclude from consideration the 1-pair of processors connected by that arc, thereby decreasing T^* by 1. In such a case, the states of processors with $w \geq 2$ will be determined, except for the special case in which, after excluding the 1-pair, no connections with test result "0" remain in the ?-chain at all. Therefore, a ?-chain of the greatest possible length must either consist exclusively of arcs with test result "1", or have such a structure that no "0" connections remain after the exclusion of any 1-pair from consideration.

It is not difficult to see that the greatest possible length for which a ?-chain c satisfies these requirements is $l(c) = 4$.

Let us list all possible variants of such a ?-chain:

$$1.\left[X \overset{1}{\rightarrow}\right] L_0 \underset{1}{\overset{1}{\rightarrow}} L_1 \underset{1}{\overset{1}{\rightarrow}} L_2 \underset{1}{\overset{1}{\rightarrow}} L_3$$
$$2.\left[X \overset{1}{\rightarrow}\right] L_0 \underset{1}{\overset{1}{\rightarrow}} L_1 \underset{1}{\overset{0}{\rightarrow}} L_2 \underset{2}{\overset{1}{\rightarrow}} L_3$$
$$3.\left[X \overset{1}{\rightarrow}\right] L_0 \underset{1}{\overset{0}{\rightarrow}} L_1 \underset{2}{\overset{1}{\rightarrow}} L_2 \underset{1}{\overset{0}{\rightarrow}} L_3.$$

Neither of the listed variants makes it possible to determine the state of any processor, since excluding any 1-pair leaves no processor with $w \geq 2$. Each of these variants requires the use of both as-yet-undetected 1-processors, and it is impossible to add one more 0-processor to any of them: regardless of the position chosen for the additional 0-processor, either an additional connection with test result "0" will be formed, and therefore some processor will retain weight $w \geq 2$ after the exclusion of a certain 1-pair, or it will become possible to exclude two 1-pairs simultaneously, reducing T^* to zero and therefore determining the states of all processors with $w \geq 1$, that is, all processors not excluded from consideration.

Therefore, $l(c) \leq 4$.

It is known that the formation of ?-subgraphs with $d^u \leq 1$ is impossible (**Theorem 2**). Therefore, for $T = 4$ and $n_1 = 2$, only the cases $2 \leq d^u \leq 4$ must be considered.

Theorem 6. A ?-subgraph with $d^u = 2$ can exist for $T^* = 2$ only if it contains a single ?-processor.

Proof. The existence of a ?-subgraph with $d^u = 2$ is possible only if each of the two 1-processors provides exactly one incoming connection (**Theorem 4**).

Let the 1-processors be denoted as X_0 and X_1. The existence of a ?-subgraph with $d^u = 2$ then requires the formation of two ?-chains, L and R, together with the corresponding sets of processors belonging to them, described as follows:

$$L_0 \equiv X_0 + S_1 \bmod n$$
$$R_0 \equiv X_1 + S_2 \bmod n$$
$$L = R, \{X_0, X_1\} \cap L = \emptyset.$$

I.e., the sets L and R are equal: both ?-chains contain the same set of processors, although these processors occur in a different order in each chain. Together, the two ?-chains form the corresponding ?-subgraph. The ?-subgraph cannot contain any additional ?-chains, since this would require conditions analogous to those arising in the case $d^u \leq 1$, which has already been shown to be impossible [28]. Consequently, each of the two chains must indeed contain all processors belonging to the ?-subgraph.

According to **Theorem 5**, $1 \leq l(L, R) \leq 4$.

The case of a ?-subgraph whose ?-chains have length $l = 1$ was demonstrated in the same theorem. Such a ?-subgraph can indeed exist.

The $l = 2$ case is impossible, since there are only two possible orderings of two processors within a ?-chain. Assuming that such chains L and R exist results in the formation of a reciprocal connection, which is not admissible:

$$L\colon [X_0 \rightarrow] L_0 \rightarrow L_1$$
$$R\colon [X_1 \rightarrow] L_1 \rightarrow L_0.$$

The $l = 3$ case permits six possible processor orderings. Let L: L_0, L_1, L_2. Then none of the five remaining possible orderings can be used to form the chain R (Table 1).

Therefore, only the case $l = 4$ remains to be considered.

Table 1. **Impossibility of forming the ?-chain *R* for each possible processor ordering**

R	Reason for impossibility
L_0, L_2, L_1	Reciprocal arc L_1–L_2
L_1, L_0, L_2	Reciprocal arc L_0–L_1
L_1, L_2, L_0	Multiple arc L_1–L_2
L_2, L_0, L_1	Multiple arc L_0–L_1
L_2, L_1, L_0	Reciprocal arcs L_0–L_1, L_1–L_2

Source: **compiled by the authors**

By similarly excluding all $l = 4$ processor orderings that would require the occurrence of

multiple or reciprocal arcs, the following admissible ?-chains are obtained:

$$L: [X_0 \to] L_0 \to L_1 \to L_2 \to L_3$$
$$R^1: [X_1 \to] L_1 \to L_3 \to L_0 \to L_2$$
$$R^2: [X_1 \to] L_2 \to L_0 \to L_3 \to L_1.$$

Let us analyze the restrictions imposed on the diagnostic graph by these ?-chains. For the R^1 case, we obtain:

$$R = R^1: [X_1 \to] L_1 \to L_3 \to L_0 \to L_2$$
$$L_0 \equiv X_0 + S_1 \equiv X_1 + 3S_2 \Rightarrow X_0 \equiv X_1 + 3S_2 - S_1$$
$$L_1 \equiv X_0 + 2S_1 \equiv X_1 + S_2 \Rightarrow X_1 \equiv X_0 + 2S_1 - S_2$$
$$L_2 \equiv X_0 + 3S_1 \equiv X_1 + 4S_2 \Rightarrow X_0 \equiv X_1 + 4S_2 - 3S_1$$

$$X_1 + 3S_2 - S_1 \equiv X_1 + 4S_2 - 3S_1 \Rightarrow S_2 \equiv 2S_1$$
$$X_0 \equiv X_0 + 2S_1 - S_2 + 3S_2 - S_1 \Rightarrow S_1 \equiv -2S_2$$
$$S_1 \equiv -2 \cdot 2S_1 \equiv -4S_1$$
$$5S_1 \equiv 0 \bmod n.$$

For the R^2 case, we obtain:

$$R = R^2: [X_1 \to] L_2 \to L_0 \to L_3 \to L_1$$
$$L_0 \equiv X_0 + S_1 \equiv X_1 + 2S_2 \Rightarrow X_0 \equiv X_1 + 2S_2 - S_1$$
$$L_1 \equiv X_0 + 2S_1 \equiv X_1 + 4S_2 \Rightarrow X_1 \equiv X_0 + 2S_1 - 4S_2$$
$$L_2 \equiv X_0 + 3S_1 \equiv X_1 + S_2 \Rightarrow X_0 \equiv X_1 + S_2 - 3S_1$$

$$X_1 + 2S_2 - S_1 \equiv X_1 + S_2 - 3S_1 \Rightarrow S_2 \equiv -2S_1$$
$$X_0 \equiv X_0 + 2S_1 - 4S_2 + 2S_2 - S_1 \Rightarrow S_1 \equiv 2S_2$$
$$S_1 \equiv -2 \cdot 2S_1 \equiv -4S_1$$
$$5S_1 \equiv 0 \bmod n.$$

Thus, to permit the formation of either of the possible chains *R*, the diagnostic graph of the FTMS must satisfy the following condition:

$$5S_1 \equiv 0 \bmod n \Rightarrow 5S_1 = kn, k \in \mathbb{Z}$$
$$S_1 = k\frac{n}{5}, \ \ k, \frac{n}{5} \in \mathbb{Z}.$$

However, this condition implies that:

$$S_2 = \pm 2S_1 = \pm 2k\frac{n}{5}$$
$$\gcd(n, S_1, S_2) = \frac{n}{5}.$$

This contradicts one of the fundamental assumptions of the problem, since for $\gcd(n, S_1, S_2) \neq 1$ the diagnostic graph is not connected.

An example of such a graph is presented in Fig. 2. As can be seen, the graph is disconnected and consists of two connected components of order 5 each. One of these components remains entirely ambiguous, since it violates the diagnosability condition $n \geq 2T + 1$.

Thus, it has been proved that, for $T^* = 2$, a ?-subgraph with $d^u = 2$ can exist only if it contains a single ?-processor.

Theorem 7. For $n_1 = 2$ and $T^* = 2$, an FTMS may contain two ?-subgraphs with $d^u = 2$ only if $S_1 \equiv S_2 \bmod \frac{n}{2}$ (or, equivalently, $S_2 = S_1 + \frac{n}{2}$).

Proof. It is already known that a single subgraph with $d^u = 2$ may exist (**Theorem 6**), and that such a subgraph contains only one ?-processor. Since, in an FTMS with $n_1 = 2$, four 1-connections are available, it is possible to consider the existence of two such ?-subgraphs and, accordingly, total $n_? = 2$.

Let the 1-processors be denoted as X_0 and X_1. Then, for the existence of two ?-subgraphs with $l = 1$, it is necessary that both 1-processors be predecessors of both ?-processors, but via different jumps.

That is,

$$X_0 + S_1 \equiv X_1 + S_2, \qquad X_0 + S_2 \equiv X_1 + S_1$$
$$X_0 \equiv X_1 + S_2 - S_1, \qquad X_1 \equiv X_0 + S_2 - S_1$$
$$X_0 \equiv (X_0 + S_2 - S_1) + S_2 - S_1 \Rightarrow 2S_2 \equiv 2S_1.$$

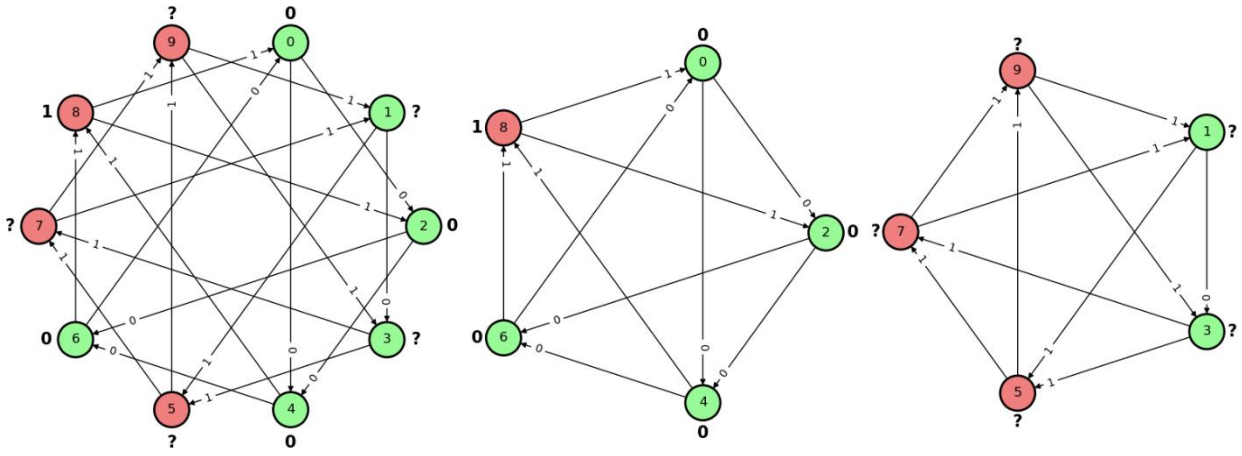


Fig. 2. **Example of the diagnostic graph *G*(10, 2, 4) satisfying the condition $S_1 = k\frac{n}{5}$**

Source: **compiled by the authors**

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

$$2S_1 - 2S_2 \equiv 0 \bmod n \Rightarrow 2S_1 - 2S_2 = kn, k \in \mathbb{Z}$$
$$S_1 \equiv S_2 \bmod \frac{n}{2}, \frac{n}{2} \in \mathbb{Z}.$$

The difference of two even numbers is always even; therefore, kn must also be even for this equality to hold. The use of $S_{1,2} \geq n$ is meaningless for the problem considered, therefore $|S_1 - S_2| < n$, $|2S_1 - 2S_2| < 2n$, which implies $|k| = 1$. Thus, we see that two ?-subgraphs with $l = 1$ can indeed exist. For this, it is necessary that n be even and that $S_1 \equiv S_2 \bmod \frac{n}{2}$, which may be simplified to $S_2 = S_1 + \frac{n}{2}$.

An example of such a graph is shown in Fig. 3. It can be seen that two ?-subgraphs are formed, each containing a single ?-processor: {4} and {9}.

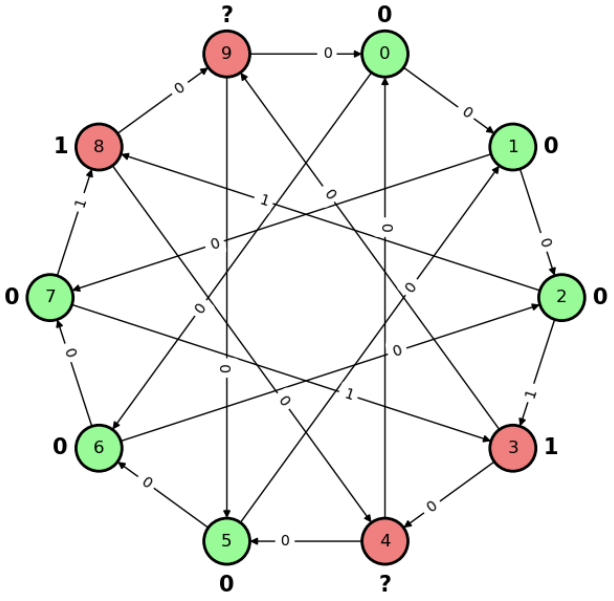


Fig. 3. **Example of the diagnostic graph $G(10, 1, 6)$ satisfying the condition $S_2 = S_1 + \frac{n}{2}$**

Source: **compiled by the authors**

It is interesting to note that, in this same case, if the outgoing connections of the ?-processors have test result "1", a single ?-subgraph with $n_? = 4$, $d^u = 4$ is formed (see Fig. 4). One may therefore hypothesize that the condition $S_2 = S_1 + \frac{n}{2}$ is also a sufficient condition for the existence of at least one arrangement of processors and test results, within admissible configurations, with $n_? = 4$. However, this assumption requires additional investigation and analysis.

Of further interest is the fact that the same condition (denoted as $2S_1 \equiv 2S_2 \bmod n$, which is equivalent) has been shown to allow two ambiguities in $T = 3$ systems, per [27].

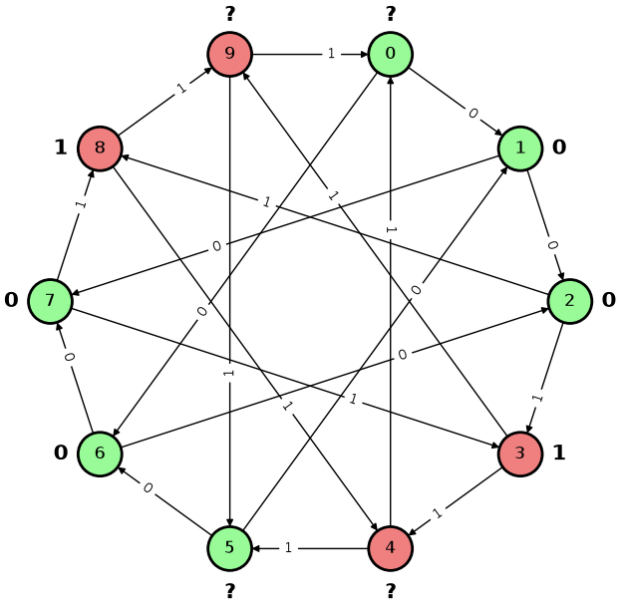


Fig. 4. **Example of the diagnostic graph $G(10, 1, 6)$ exhibiting one $d^u = 4$?-subgraph with four ambiguities**

Source: **compiled by the authors**

DISCUSSION OF RESULTS

The obtained results provide a more detailed description of the structure of ambiguities arising in the $T = 4$, $n_1 = 2$ case. Previous studies established general restrictions on the number of ambiguous processors, identified the basic conditions governing the existence of ?-subgraphs and ?-chains, and demonstrated configurations in which the number of ambiguities may approach the maximum admissible value [27], [28]. In contrast to those results, the present study focuses not only on the overall number of ambiguous processors, but also on the internal structure of an individual ambiguity region and on the relationship between that structure and the parameters of the diagnostic graph.

The established upper bound on the length of a ?-chain shows that, for $T^* = 2$, an ambiguity region cannot propagate indefinitely along either of the jumps of the circulant. This restriction results from the interaction of two mechanisms employed by the testing procedure: the accumulation of processor weights within sequences of connections having test result "0", and the reduction of T^* following the exclusion of a 1-pair. When the length of a chain exceeds four, at least one of these mechanisms leads to the determination of the states of some processors and, consequently, to the interruption of the ?-chain. Thus, the obtained restriction is not merely combinatorial in nature, but also directly reflects the operational logic of the self-testing method under consideration.

The result concerning a ?-subgraph with $d^u = 2$ further strengthens this restriction. The minimum admissible number of incoming 1-connections cannot sustain a connected ambiguity region containing several ?-processors: such a ?-subgraph necessarily degenerates into a single vertex.

Attempts to construct a multi-vertex subgraph of this type result either in the formation of multiple or bidirectional arcs, which are prohibited by the assumptions of the problem, or in relations among *n*, S_1, and S_2 that are incompatible with the strong connectivity of the circulant.

The graph presented in Fig. 2 illustrates the latter case: the configuration required for the existence of a multi-vertex ?-subgraph causes the diagnostic graph to decompose into separate connected components. Consequently, the strong-connectivity requirement serves not only as an initial constraint of the model, but also as one of the factors that localize the possible ambiguity regions.

At the same time, the local nature of an individual ?-subgraph with $d^u = 2$ does not exclude the simultaneous occurrence of several independent ambiguity regions. The established condition $S_2 = S_1 + \frac{n}{2}$ shows that the occurrence of two such subgraphs is associated with a particular symmetry of the circulant: the two jumps differ by half the order of the graph, and the corresponding pairs of vertices therefore occupy mutually opposite positions.

The example $G(10,1,6)$ presented in Fig. 3 confirms that a configuration containing two isolated ?-processors is attainable. From a practical perspective, this means that the relationship between the jumps may be used as a criterion for the preliminary analysis of a diagnostic topology. Avoiding the relation $S_2 = S_1 + \frac{n}{2}$ excludes the considered mechanism by which two ?-subgraphs with $d^u = 2$ may arise simultaneously.

Nevertheless, the examples presented above demonstrate that the topology parameters do not definitively determine the number of ambiguities. In a graph with the same values of *n*, S_1, and S_2, a change in the test results assigned to the outgoing connections of the ?-processors may cause separate ambiguity regions to merge and may lead to the occurrence of four ambiguous-state processors, as demonstrated in Fig. 4. Therefore, the relation $S_2 = S_1 + \frac{n}{2}$ should be regarded as a structural prerequisite for the occurrence of the corresponding configurations, but not as a sufficient description of the behavior of the testing procedure for all possible arrangements of processors and test outcomes. The hypothesis that this condition is sufficient for the existence of at least one such arrangement exhibiting $n_? = 4$ requires a separate proof.

Separately, this same condition was shown [27] to allow two ambiguities in $T = 3$ systems, suggesting potential unique features of these configurations in particular.

The practical significance of the obtained results lies primarily in the possibility of reducing the set of configurations and arrangements that must be examined during the design of a diagnostic topology or during the final stages of the self-testing procedure. Once a ?-subgraph with two incoming 1-connections has been identified, there is no need to treat it as a potentially branched ambiguity region, since under the adopted assumptions it may contain only one processor. Similarly, checking the relationship between the jumps makes it possible to determine in advance whether two such regions can exist simultaneously. However, the quantitative reduction in the number of additional tests or in the computational complexity of the diagnostic procedure was not evaluated in the present study. Therefore, the corresponding practical benefit is theoretically substantiated but has not yet been measured experimentally.

It can, however, be demonstrated that exclusion of system configurations according to the obtained conditions constrains the scope of potential ambiguity cases. Consider an $n = 10, T = 4$ system. There are $\binom{9}{2} = 36$ possible distinct unordered pairs of nonzero jumps for this system, of which 20 define admissible two-jump circulants (strongly connected, no reciprocal arcs). Among these 20 admissible configurations, only four satisfy $S_1 \equiv S_2 \bmod \frac{n}{2}$. These can be enumerated explicitly: (1, 6); (2, 7); (3, 8); (4, 9). Thus, only 4 of the 20 admissible configurations satisfy the necessary condition for the occurrence of two distinct ?-subgraphs with $d^u = 2$; the remaining 16 cannot manifest this case. Furthermore, since $\frac{n}{2}$ is an essential part of the condition, this case cannot occur for odd *n*.

The limitations of the obtained results are determined by the assumptions adopted in the study. Only strongly connected directed circulants with two jumps within the framework of the PMC model were considered, while the detailed analysis was performed specifically for $T = 4$, $n_1 = 2$ (and thus $T^* = 2$), and $d^u = 2$. The established theorems cannot be directly extended to circulants with a larger number of jumps, irregular diagnostic graphs, or alternative testing models.

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

Within the chosen model and established restrictions, however, the individual results differ in their potential for generalization. The specific upper bound on ?-chain length established in **Theorem 5** follows directly from the value of T^* (the number of faults that remain admissible at the considered stage of the diagnostic procedure) and operational logic of the considered testing procedure and therefore remains applicable for arbitrary *n*, *T* and admissible choice of two jumps, provided that $T^* = 2$ faults remain undiscovered. **Theorem 6** builds upon **Theorem 5** and shares its restrictions and potential for generalization. The jump relation obtained in **Theorem 7** is only proved here under the additional condition of $n_1 = 2$, which, together with $T^* = 2$, corresponds to the considered case $T = 4$, making the obtained result local to this case. It should be noted, however, that the occurrence of the same relation in the previously investigated case [27] suggests that it may represent a more general structural property of two-jump circulant diagnostic graphs. Establishing the range of fault parameters for which this relation remains applicable requires separate investigation.

Furthermore, the $d^u = 3$ and $d^u = 4$ scenarios remain outside of the scope of the analysis. Investigation of these scenarios is necessary to complete the structural description of the $T = 4$ case, establish corresponding bounds on the number of ambiguous processors for this case, and to determine whether the identified jump symmetry is a specific property of the $d^u = 2$ scenario or a manifestation of a more general structural regularity.

The investigation of the $T = 4$ case in particular is of considerable practical importance in the context of real-world applications, where $T \leq 4$ is commonly observed. Consequently, a complete description of the $T = 4$ case, considered together with the results of previous studies addressing $T < 4$, would substantially expand the practical possibilities for bounding the number of ambiguities that may arise in fault-tolerant multiprocessor systems.

CONCLUSIONS

The study investigated the conditions under which ambiguities arise during the self-testing of fault-tolerant multiprocessor systems whose diagnostic graphs are represented by strongly connected directed circulants with two jumps. Based on the previously introduced concepts of ?-subgraphs and ?-chains, an analysis was performed for individual scenarios with $d^u = 2$ within the $T = 4$ case that had not been examined in earlier studies. As a result, the set of configurations that remain unexplored for this case has been substantially reduced.

It was proved that, for $T^* = 2$, the length of a ?-chain is bounded by four vertices. It was also established that a ?-subgraph with two incoming 1-connections may contain only a single processor whose state remains ambiguous. Furthermore, the condition under which two independent ?-subgraphs of this type may exist was determined, namely the following relationship between the jumps of the circulant: $S_2 = S_1 + \frac{n}{2}$

The obtained results provide a more precise description of the structure of possible ambiguities arising during the self-testing procedure and reduce the set of configurations in which the occurrence of a particular number of ambiguities is fundamentally possible. The theoretical significance of the results lies in bringing the structural description of the case $T = 4$ closer to completion. The practical significance of the study lies in the possibility of using the established regularities to further improve FTMS diagnostic methods and reduce the number of additional tests required within such methods to resolve the remaining ambiguities.

Promising directions for further research include verifying the hypothesis that the condition $S_2 = S_1 + \frac{n}{2}$ permits occurrence of four ambiguities, which has not been proved in the present study; analyzing the scenarios $d^u = 3$ and $d^u = 4$, which would complete the structural description of the $T = 4$ case, and extending the obtained results to cases involving other admissible numbers of faults.

Conflict of interests: Authors declare that they do not have conflict of interests, in particular financial, personal, copyright or any of a different nature, which could have influenced the research, as well as the results published in this article

Financing: Research was carried out without financial support

Accessibility data: All data available in digital or graphic form in the main text manuscript

Using artificial intelligence tools: During the preparation of the manuscript, the ChatGPT-5.6 Sol (OpenAI, August 2026) artificial intelligence (AI) tool was used for grammatical and stylistic text checks. All fragments processed by it were validated and edited by the authors. AI was not used to generate text, formulas, and tables, nor to form scientific provisions, derive results or conclusions. Scientific provisions, results and conclusions are the authors' own intellectual contributions

REFERENCES

1. Perez Cerrolaza, J., Obermaisser, R., Abella Ferrer, J., Cazorla Almeida, F. J., Grüttner, K., Agirre, I., Ahmadian, H. & Allende, I. "Multi-core devices for safety-critical systems: a survey". *ACM Computing Surveys*. 2020; 53 (4): 79. DOI: https://doi.org/10.1145/3398665.

2. Heidari Iman, M. R. & Pejman, Y. "A software control flow checking technique in multi-core processors". *International Journal of Embedded Systems*. 2020; 13 (2): 136–147. DOI: https://doi.org/10.1504/IJES.2020.108861.

3. Kotov, D. O. "A generalized model of an adaptive information-control system of a car with multi-sensor channels of information interaction". *Applied Aspects of Information Technology*. 2021; 5 (1): 25–34. DOI: https://doi.org/10.15276/aait.05.2022.2.

4. Antoniuk, V. V., Drozd, M. O. & Drozd, O. B. "Power-oriented checkability and monitoring of the current consumption in FPGA projects of the critical applications". *Applied Aspects of Information Technology*. 2019; 2 (2): 105–114. DOI: https://doi.org/10.15276/aait.02.2019.2.

5. Nazarova, O. S., Osadchyy, V. V. & Rudim, B. Y. "Computer simulation of the microprocessor liquid level automatic control system". *Applied Aspects of Information Technology*. 2023; 6 (2): 163–174. DOI: https://doi.org/10.15276/aait.06.2023.12.

6. Kalel, D. & Singh, R. R. "IoT integrated adaptive fault tolerant control for induction motor based critical load applications". *Engineering Science and Technology, an International Journal*. 2024; 51: 101585, https://www.sciencedirect.com/science/article/pii/S221509862300263X.
DOI: https://doi.org/10.1016/j.jestch.2023.101585.

7. Leveson, N. G. "Engineering a Safer World: Systems Thinking Applied to Safety". *MIT Press*. 2012. DOI: https://doi.org/10.7551/mitpress/8179.001.0001.

8. Kovalev, I. S., Drozd, O. V., Rucinski, A., Drozd, M. O., Antoniuk, V. V. & Sulima, Y. Y. "Development of computer system components in critical applications: problems, their origins and solutions". *Herald of Advanced Information Technology*. 2020; 3 (4): 252–262. DOI: https://doi.org/10.15276/hait.04.2020.4.

9. Godabole, P. & Bhole, G. "Utilization and criticality based fault-tolerant scheduling in multicore mixed critical systems". *International Journal of Pervasive Computing and Communications*. 2024; 20 (1): 126–146, https://www.scopus.com/record/display.uri?eid=2-s2.0-85149644279&origin=resultslist. DOI: https://doi.org/10.1108/IJPCC-06-2022-0248.

10. Qin, W., Tang, W. & Xia, W. "Robust fault-tolerant control based on set-membership estimation and tube MPC". *IEEE Transactions on Automation Science and Engineering*. 2025; 22: 19499–19510. DOI: https://doi.org/10.1109/TASE.2025.3594583.

11. Joshi, H. & Sinha, N. K. "Adaptive fault tolerant control design for stratospheric airship with actuator faults". *IFAC-PapersOnLine*. 2022; 55 (1): 819–825, https://www.scopus.com/record/display.uri?eid=2-s2.0-85132157930&origin=resultslist. DOI: https://doi.org/10.1016/j.ifacol.2022.04.134.

12. Fang, Y., Lu, Y., Han, T. & Hu, Q. "Design of missile incremental adaptive fault tolerant control system". *Journal of Beijing University of Aeronautics and Astronautics*. 2022; 48 (5): 920–928, https://www.scopus.com/record/display.uri?eid=2-s2.0-85130918044&origin=reflist.
DOI: https://doi.org/10.13700/j.bh.1001-5965.2021.0454.

13. Hu, Q., Niu, G. & Wang, C. "Spacecraft attitude fault-tolerant control based on iterative learning observer and control allocation". *Control Allocation for Spacecraft under Actuator Faults*. 2018; 75: 245–253, https://www.scopus.com/record/display.uri?eid=2-s2.0-85041462830&origin=resultslist. DOI: https://doi.org/10.1016/j.ast.2017.12.031.

14. Myrnneko, M. D. & Shevel, V. V. "Technological platforms, tools, and standardization in the unified information space for automated unmanned aerial vehicle design". *Applied Aspects of Information Technology*. 2025; 8 (3): 316–333. DOI: https://doi.org/10.15276/aait.08.2025.21.

15. Hu, B. & Seiler, P. "Pivotal decomposition for reliability analysis of fault tolerant control systems on unmanned aerial vehicles". *Reliability Engineering & System Safety*. 2015; 140: 130–141, https://www.scopus.com/pages/publications/84928741612. DOI: https://doi.org/10.1016/j.ress.2015.04.005.

16. Zhao, Y., Wu, Z., Li, F., Yang, T., Yang, C. & Gui, W. "Design and implementation of fuzzy-mode-based fault isolation and fault-tolerant control for aircraft electric braking systems". *IEEE*

Transactions on Automation Science and Engineering. 2025; 22: 12297–12308. DOI: https://doi.org/10.1109/TASE.2025.3543647.

17. Romankevich, V. A. "Self-testing of multiprocessor systems with regular diagnostic connections". *Automation and Remote Control.* 2017; 78 (2): 289−299. DOI: https://doi.org/10.1134/S0005117917020084.

18. Preparata, F. P., Metze, G. & Chien, R. T. "On the connection assignment problem of diagnosable systems". *IEEE Transactions on Electronic Computers*. 1967; EC-16 (6): 848−854. DOI: https://doi.org/10.1109/PGEC.1967.264748.

19. Liu, J., Zhou, Q., Yu, Zh. & Zhou, Sh. "Fault diagnosability of regular networks under the hybrid PMC model". *Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics)*. 2021; 13025 (LNCS): 283–297, https://www.scopus.com/record/display.uri?eid=2-s2.0-85118183684&origin=resultslist. DOI: https://doi.org/10.1007/978-3-030-89543-3_24.

20. Mánik, M. & Gramatová, E. "Diagnosis of faulty units in regular graphs under the PMC model". *Proceedings of the 2009 12th International Symposium on Design and Diagnostics of Electronic Circuits & Systems*. 2009: 202–205, https://www.scopus.com/record/display.uri?eid=2-s2.0-70349337043&origin=resultslist. DOI: https://doi.org/10.1109/DDECS.2009.5012128.

21. Chang, N.-W. & Hsieh, S.-Y. "Conditional diagnosability of alternating group networks under the PMC model". *IEEE/ACM Transactions on Networking*. 2020; 28 (5): 1968–1980, https://www.scopus.com/record/display.uri?eid=2-s2.0-85105805249&origin=resultslist. DOI: https://doi.org/10.1109/TNET.2020.3002093.

22. Abbaspour, A., Mokhtari, S., Sargolzaei, A. & Yen, K. K. "A survey on active fault-tolerant control systems". *Electronics*. 2020; 9 (9): 1–23, https://www.scopus.com/record/display.uri?eid=2-s2.0-85090902832&origin=resultslist. DOI: https://doi.org/10.3390/electronics9091513.

23. Pathan, R. M. "Fault-tolerant and real-time scheduling for mixed-criticality systems". *Real-Time Systems*. 2014; 50 (4): 509–547, https://www.scopus.com/record/display.uri?eid=2-s2.0-84903574751&origin=reflist. DOI: https://doi.org/10.1007/s11241-014-9202-z.

24. Safari, S. et al. "A survey of fault-tolerance techniques for embedded systems from the perspective of power, energy, and thermal issues". *IEEE Access*. 2022; 10: 12229–12251, https://www.scopus.com/record/display.uri?eid=2-s2.0-85123365684&origin=resultslist. DOI: https://doi.org/10.1109/ACCESS.2022.3144217.

25. Nedeljkovic, J. N., Dosic, S. M. & Nikolic, G. S. "A survey of hardware fault tolerance techniques". *2023 58th International Scientific Conference on Information, Communication and Energy Systems and Technologies (ICEST). Proceedings*. 2023. p. 223–226, https://www.scopus.com/record/display.uri?eid=2-s2.0-85167870342&origin=resultslist. DOI: https://doi.org/10.1109/ICEST58410.2023.10187275.

26. Mithun, B., Laxman, S., Gour, K. D. & Kalishankar, T. "Fault-tolerant metric dimension of circulant graphs Cn(1,2,3)". *Theoretical Computer Science*. 2020; 817: 66–79, https://www.scopus.com/record/display.uri?eid=2-s2.0-85060525332&origin=resultslist. DOI: https://doi.org/10.1016/j.tcs.2019.01.011.

27. Romankevich, V. A., Morozov, K. V., Romankevich, O. V. & Zacharioudakis, L. "Ambiguities and their emergence conditions in self-testing of multiprocessor systems". *Herald of Advanced Information Technology*. 2024; 7 (4): 405−413. DOI: https://doi.org/10.15276/hait.07.2024.29.

28. Romankevich, V., Melnyk, O., Morozov, K., Romankevich, A. & Yermolenko, I. "Conditions for the emergence of ambiguities in testing of fault-tolerant multiprocessor systems". *Information Technology: Computer Science, Software Engineering and Cyber Security.* 2026; 1: 146–154. DOI: https://doi.org/10.32782/IT/2026-1-16.

Received 02.09.2026
Received after revision 22.10.2026
Accepted 30.10.2026

DOI: https://doi.org/10.15276/aait.09.2026.45
UDC 004.052

Структурний аналіз ситуацій з виникненням невизначеностей при самотестуванні відмовостійких багатопроцесорних систем

Романкевич Віталій Олексійович[1)]
ORCID: https://orcid.org/0000-0003-4696-5935; zavkaf@scs.kpi.ua. Scopus Author ID: 57193263058
Мельник Олександр Олегович[1)]
ORCID: https://orcid.org/0009-0003-7527-8146; inboxnumberzero@zoho.com
Романкевич Олексій Михайлович[1)]
ORCID: https://orcid.org/0000-0001-5634-8469; romankev@scs.kpi.ua. Scopus Author ID: 6602114176
Морозов Костянтин В'ячеславович[1)]
ORCID: https://orcid.org/0000-0003-0978-6292; mcng@ukr.net. Scopus Author ID: 57222509251
Захаріудакіс Лефтеріс[2)]
ORCID: https://orcid.org/0000-0002-9658-3073; l.zacharioudakis@nup.ac.cy. Scopus Author ID: 57422876200
[1)] Національний технічний університет України "Київський політехнічний інститут імені Ігоря Сікорського", пр. Берестейський, 37. Київ, 03056, Україна
[2)] Університет Неаполіс Пафос, Данаіс Авеню, 2, Пафос, 8042, Кіпр

АНОТАЦІЯ

Актуальність дослідження зумовлена необхідністю підвищення надійності та ефективності процедур самотестування відмовостійких багатопроцесорних систем. Існуючі підходи, що базуються на мінімальній множині діагностичних зв'язків, можуть залишати стани деяких процесорів невизначеними, що потребує виконання додаткових перевірок. **Метою** роботи є уточнення структурного опису формування невизначеностей у системах, діагностичний граф яких є сильно зв'язним орієнтованим циркулянтом із двома стрибками. **Завдання** включають визначення раніше невідомих обмежень на структуру ?-ланцюжків та ?-підграфів, визначення умов існування таких підграфів із мінімально допустимою кількістю вхідних зв'язків відмови, а також встановлення умов, за яких у системі можуть виникати декілька незалежних підграфів. **Методи.** Використано методи теорії графів, аналіз співвідношень параметрів циркулянтів за модулем, структурну декомпозицію областей невизначеності та повний перебір допустимих конфігурацій ?-ланцюжків. **Результати** встановлюють скінченну верхню межу довжини ?-ланцюжка для розглянутого стану залишкових невизначеностей. Доведено, що ?-підграф з мінімально допустимою кількістю вхідних зв'язків відмови може містити лише один процесор у невизначеному стані. Також встановлено необхідне співвідношення між стрибками циркулянта, за якого можливе одночасне існування двох незалежних ?-підграфів такого типу. **Наукова новизна** полягає в розширенні структурної теорії виникнення невизначеностей для розглянутої кількості несправностей і суттєвому звуженні множини конфігурацій, що потребують подальшого аналізу. **Практична цінність** результатів полягає в можливості їх застосування для вдосконалення алгоритмів самотестування, виключення неможливих конфігурацій невизначеності та скорочення кількості додаткових діагностичних перевірок, необхідних для визначення станів процесорів.

Ключові слова: відмовостійка багатопроцесорна система; самотестування; діагностичний граф; орієнтований циркулянт; невизначений стан процесора

ABOUT THE AUTHORS



Vitaliy A. Romankevich - Doctor of Engineering Sciences, Professor, Head of System Programming and Specialized Computer System Department. National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute", 37, Beresteiskyi Ave, Kyiv, 03056, Ukraine
ORCID: https://orcid.org/0000-0003-4696-5935; zavkaf@scs.kpi.ua. Scopus Author ID: 57193263058
***Research field*:** Fault-tolerant multiprocessor systems reliability estimation; GL-models; Self-diagnosable systems; Diagnosis of multiprocessor systems; Discrete mathematics

Романкевич Віталій Олексійович - доктор технічних наук, професор, завідувач кафедри Системного програмування і спеціалізованих комп'ютерних систем. Національний технічний університет України "Київський політехнічний інститут імені Ігоря Сікорського", пр. Берестейський, 37. Київ, 03056, Україна
***Галузь досліджень*:** оцінка надійності відмовостійких багатопроцесорних систем; GL-моделі; самодіагностовні системи; діагностика багатопроцесорних систем; дискретна математика



Oleksandr O. Melnyk - postgraduate student, System Programming and Special Computer System Department. National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute", 37, Beresteiskyi Ave. Kyiv, 03056, Ukraine
ORCID: https://orcid.org/0009-0003-7527-8146; inboxnumberzero@zoho.com
Research field: Fault-tolerant multiprocessor system reliability estimation; Self-diagnosable multiprocessor systems

Мельник Олександр Олегович - аспірант, кафедри Системного програмування і спеціалізованих комп'ютерних систем. Національний технічний університет України "Київський політехнічний інститут імені Ігоря Сікорського", пр. Берестейський, 37. Київ, 03056, Україна
Галузь досліджень: оцінка надійності відмовостійких багатопроцесорних систем; самодіагностовні багатопроцесорні системи



Alexei M. Romankevich - Doctor of Engineering Sciences, Professor, System Programming and Specialized Computer System Department. National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute", 37, Beresteiskyi Ave, Kyiv, 03056, Ukraine
ORCID: https://orcid.org/0000-0001-5634-8469; romankev@scs.kpi.ua. Scopus Author ID: 6602114176
***Research field*:** Fault-tolerant multiprocessor systems reliability estimation; GL-models; Self-diagnosable systems; Diagnosis of multiprocessor systems; Multi-valued logic

Романкевич Олексій Михайлович - доктор технічних наук, професор, кафедра Системного програмування і спеціалізованих комп'ютерних систем. Національний технічний університет України "Київський політехнічний інститут імені Ігоря Сікорського", пр. Берестейський, 37. Київ, 03056, Україна
***Галузь досліджень*:** оцінка надійності відмовостійких багатопроцесорних систем; GL-моделі; самодіагностовні системи; діагностика багатопроцесорних систем; багатозначна логіка



Kostiantyn V. Morozov - PhD, Associate Professor, System Programming and Specialized Computer System Department. National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute", 37, Beresteiskyi Ave. Kyiv, 03056, Ukraine
ORCID: https://orcid.org/0000-0003-0978-6292, mcng@ukr.net, Scopus Author ID: 57222509251
***Research field*:** GL-models; Fault-tolerant multiprocessor systems reliability estimation; Self-diagnosable multiprocessor systems

Морозов Костянтин В'ячеславович - кандидат технічних наук, доцент кафедри Системного програмування і спеціалізованих комп'ютерних систем. Національний технічний університет України "Київський політехнічний інститут імені Ігоря Сікорського", пр. Берестейський, 37. Київ, 03056, Україна
***Галузь досліджень*:** GL-моделі; оцінка надійності відмовостійких багатопроцесорних систем; самодіагностовні багатопроцесорні системи



Lefteris Zacharioudakis - PhD (Eng), Assistant professor, Neapolis University Pafos, 2, Danais Ave. Pafos, 8042, Cyprus
ORCID: https://orcid.org/0000-0002-9658-3073; l.zacharioudakis@nup.ac.cy. Scopus Author ID: 57422876200
Research field: Principles of CyberSecurity, Operating systems, Information Security, Cryptography, Penetration Testing

Захаріудакіс Лефтеріс - кандидат технічних наук, доцент. Університет Неаполіс Пафос, Данаіс Авеню, 2, Пафос, 8042, Кіпр
***Галузь досліджень*:** основи кібербезпеки, операційні системи, інформаційна безпека, криптографія, тестування на проникнення